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PN - JP3100848 A 19910425
TI - MEMORY BACK-UP DEVICE USING EEPROM
FI - G06F12/16&340Q
PA - JAPAN SERVO
IN - MARUYAMA TOMOYOSHI
AP - JP19890237257 19890914
PR - JP19890237257 19890914
DT - I

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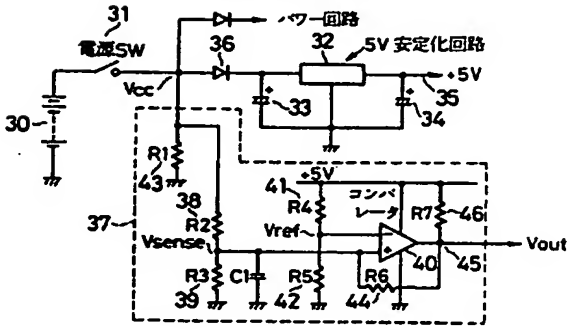
PN - JP3100848 A 19910425
TI - MEMORY BACK-UP DEVICE USING EEPROM
AB - PURPOSE:To economically back up a memory with high reliability by sending an interruption signal to a CPU after detection of the service interruption of a working power supply and actuating the CPU with the remaining electric charge of a voltage stabilizing circuit to transfer the necessary data to an EEPROM from a RAM.
- CONSTITUTION:A CPU 1 is provided together with a main control circuit where an EEPROM 20 is connected to a data bus 4 connected to a ROM 2 and a RAM 3 and an address bus 5, a stabilizing circuit 32, and a power supply circuit which is connected to a logic power supply 35 via the capacitors 33 and 34 and supplies the power to a main control circuit. Then the output of a voltage detector 37 is connected to an interruption signal terminal of the CPU 1 and a disable terminal of a control circuit 50. When the discontinuation of power supply is detected by the detector 37, an interruption signal is sent to the CPU 1 and a transfer program is actuated by the electric charge of both capacitors 33 and 34. Then the data to be stored in the capacity of the RAM 3 at that time point are selectively transferred to the EEPROM 20. Thus it is possible to obtain an economical memory back-up device with high reliability.
I - G06F12/16
PA - JAPAN SERVO CO LTD
IN - MARUYAMA TOMOYOSHI
ABD - 19910724
ABV - 015292
GR - P1230
AP - JP19890237257 19890914

符号の説明

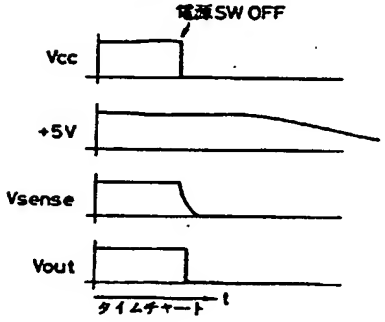
1…CPU，2…ROM，3…RAM，4…データバス，5…アドレスバス，6，35…ロジック電源，7…バックアップ用電源，8…電圧監視回路，9，10…ダイオード，11…警報回路，20…EP*ROM，30…常用電源，31…電源スイッチ，32…安定化回路，33，34…コンデンサ，36…逆流防止器，37…電圧検出器，38，39，41，42，43，44，46，53…抵抗，40…コンパレータ，45…コンパレータの出力端子，50…その他の表示装置，51…リセットスイッチ，52…パワーリセット回路，54…コンデンサ，56…ヒステリシス回路。

特許出願人　日本サーボ株式会社

第2図(a)



第2図(b)



第1図